REMARKS

Claims 1-5, 8-16 and 19-31 are pending in the application.

Claims 1-5, 8-16 and 19-31 have been rejected.

Claims 23, 24, 28 and 31have been amended solely to correct informalities.

I. CLAIM OBJECTIONS

Claims 24, 28 and 31 were objected to due to one or more minor informalities. Applicant has reviewed these claims. Claims 24 and 28 have been amended to replace the subscript "Y" with "X". Claim 31 has been amended to include a period. Upon further review of Claim 23, Applicant has amended Claim 23 to correct another informality.

II. REJECTION UNDER 35 U.S.C. § 102

Claims 1-5, 8-16 and 19-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Uya (US 4,682,303). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

At the onset, and looking at Applicant's Claim 1, Applicant respectfully submits that the Office Action is unclear in identifying which element/component of Uya meets the Applicant's claimed element of "wherein a least significant adder cell in a first one of the rows of adder cells."

First, the Office Action appears to identify P2 (inclusive of adders for bits 4-7) as the least significant adder – as the Office Action equates the C8 carryout bits of Uya as the conditional carryout bits C_X of Applicant's claims. In this case, Uya's adder P2 is not a least significant adder, since Uya's adder P1 is the least significant adder. Therefore, in the event the Office Action is basing the 102 rejection on this interpretation, Uya fails to disclose each and every element of the Applicant's claims.

Second, assuming the single-bit adder for bit 4 in Uya's multi-bit adder P2 is being interpreted by the Office Action as the "least significant adder" in the row, this adder generates the carryout bits identified in Uya as C5 (really C4) carryout bits - not the C8 carryout bits as asserted by the Office Action. In the event the Office Action is basing the 102 rejection on this interpretation, Uya's carryout bits C5 (or C9, C14 or C20) are the only carryout bits that can be properly interpreted as the Applicant's carryout bits C_X recited in the Applicant's claims. See, Uya, Figure 3, 2. It is clear from Uya's Figure 3 that the second adder (for bit 5) in the row does not propagate the C5 carryout bits through a first pass gate and a second pass gate when the first data bit A_5 and the second data bit B_5 are unequal to generate the next carryout bits (C6). Uya, Figure 3. This is expressly recited in Applicant's claims by the language generate [generating in said second adder cell] both a first conditional carry-out bit, $C_{X+1}(1)$, and a second conditional carry-out bit, $C_{X+1}(0)$ by

propagating said first conditional carry-out bit, $C_X(1)$ and said second conditional carry-out bit, $C_X(0)$ through a first pass gate and a second pass gate, respectively, when said first data bit A_{X+1} and said second data bit B_{X+1} are not equal. See, independent Claims 1, 12 and 23. These amendments were made in the Applicant's prior response with proper argument.

The Office Action further argues that Uya's logic gates 54-55 meet Applicant's first and second pass gates. In order to be consistent with the Office Action's prior interpretation of the "least significant adder cell", Uya's C26 carryout bits are propagated based on carryout bits C19 from the adder P4 -- not based on whether two data bits A and B in a second adder are unequal, and not using pass gates. The elements in Uya described in the Office Action as meeting the specific claim elements recited in Applicant's claims simply do not meet the claimed elements as they are arranged, and the Office Action's reasoning and interpretation is inconsistent with the disclosure and teachings of Uya.

Therefore, and in either scenario of interpretations, Uya fails to disclose each and every element as they are arranged in Applicant's claims.

As noted in the Applicant's specification, in one embodiment, the time critical data paths through the adder cells in each row are the dual carry paths. See, Specification, page 26, lines 16-20. Applicant utilizes pass gates (or switches) to decrease the delay in these paths. Uya does not disclose the recited elements/features in Applicant's independent claims (as amended).

Accordingly, the Applicant respectfully requests the Examiner withdraw the § 102(b) rejection of Claims 1-5, 8-16 and 19-31.

III. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckbutrus.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

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